REMARKS

Upon entry of this amendment, claims 1-8 and 13-19 and 22-25 are all the claims pending in the application. Claims 9-11, 20 and 21 have been canceled by this amendment.

I. Objections to the Drawings

The Examiner has objected to the drawings for the reasons set forth on page 2 of the Office Action. In particular, the Examiner has taken the position that Figs. 1-4 should be labeled as --Prior Art--. Applicants are submitting herewith replacement sheets for Figs. 1-4, in which the --Prior Art-- legend has been added thereto. Accordingly, Applicants kindly request that the objection be reconsidered and withdrawn.

II. Claim Rejections

Claims 1-3, 9 and 23-25 were rejected under 35 U.S.C. §102(e) as being anticipated by Koizumi et al. (US 7,015,964); claims 4-8, 10 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Koizumi et al. (US 7,015,964) in view of Satoshi et al. (JP 2000-078484); and claims 11, 20 and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Koizumi et al. (US 7,015,964) in view of Applicants Admitted Prior Art (AAPA).

Claim 1, as amended, recites the feature of an electric charge simultaneous removal unit that simultaneously outputs a readout signal and a reset signal to all of the photoelectric conversion circuits disposed in a region to be read out, wherein electric charge simultaneous removal unit includes: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a source or a drain of the first switch transistor; and a second switch transistor

that serves as a switch, wherein the second switch transistor receives an all pixel reset switch signal and an all pixel reset signal, wherein the capacitor is charged during a time period in which the all pixel reset switch signal and the all pixel reset signal are input to a gate and a drain, respectively, of the second switch transistor, and wherein, when the capacitor is charged, the reset signal is input to the drain of the first switch transistor and is output simultaneously to all of the photoelectric conversion circuits from the source of the first switch transistor. Applicants respectfully submit that Koizumi does not disclose or suggest the above-noted combination of features recited in amended claim 1.

Regarding Koizumi, Applicants note that in Fig. 1 of this reference, a pixel of a solid-state image pickup device is depicted which includes a transfer switch Q1, a reset switch Q2, a transistor Q3 acting as an amplifier, and a selection switch Q4 (see col. 4, line 60 through col. 5, line 2). As explained in Koizumi with reference to the timing charts shown in Figs. 2 and 8, a diffusion region FD is reset to the reference voltage by inputting a high level pulse such as RST to the gate of the reset switch Q2, and a photoelectric converter PD is reset by inputting a high level pulse such as TX to the gate of the transfer switch Q1 (see col. 4, lines 26-27;col. 5, lines 30-32 and col. 7, lines 13-19).

Regarding Satoshi, Applicants note that this reference discloses the use of a solid state imaging device 3 having a mechanical shutter 2 arranged thereon (see Fig. 3 and Abstract). As explained in Satoshi, exposure of the imaging device is started by simultaneously resetting all of the pixels of the imaging device 3 in the state of opening the mechanical shutter 2 (see Abstract and paragraph [0011]).

Regarding the AAPA, as shown in Fig. 3, a timing generation circuit includes a bootstrap circuit 146 that functions as a capacitor, and a transistor 148. As explained on page 3 of the specification, when electric charge is accumulated in the bootstrap circuit 146, a reset signal RSCELL is output to a reset transistor of each pixel.

Based on the foregoing description, Applicants note that while (1) Koizumi discloses the ability to input a high level pulse RST to the reset switch Q2 and a high level pulse to the gate transfer switch Q1, (2) Satoshi discloses starting exposure by simultaneously resetting all of the pixels of the imaging device 3 in the state of opening the mechanical shutter 2, and (3) the AAPA discloses the use of a capacitor and a switch transistor 148 that enables a reset signal to be output to each pixel, that the combination of Koizumi, Satoshi and the AAPA does not teach, suggest or otherwise render obvious the feature of an electric charge simultaneous removal unit that includes: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a source or a drain of the first switch transistor; and a second switch transistor that serves as a switch, wherein the second switch transistor receives an all pixel reset switch signal and an all pixel reset signal, wherein the capacitor is charged during a time period in which the all pixel reset switch signal and the all pixel reset signal are input to a gate and a drain, respectively, of the second switch transistor, and wherein, when the capacitor is charged, the reset signal is input to the drain of the first switch transistor and is output simultaneously to all of the photoelectric conversion circuits from the source of the first switch transistor, as recited in amended claim 1.

Accordingly, Applicants submit that claim 1 is patentable over the cited prior art, an indication of which is kindly requested. Claims 2-8, 24 and 25 depend from claim 1 and are

therefore considered patentable at least by virtue of their dependency.

Regarding claims 22 and 23, Applicants note that both of these claims have been amended in a similar manner as claim 1 so as to recite that the electric charge simultaneous removal unit includes: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a source or a drain of the first switch transistor; and a second switch transistor that serves as a switch, wherein the second switch transistor receives an all pixel reset switch signal and an all pixel reset signal, wherein the capacitor is charged during a time period in which the all pixel reset switch signal and the all pixel reset signal are input to a gate and a drain, respectively, of the second switch transistor, and wherein, when the capacitor is charged, the reset signal is input to the drain of the first switch transistor and is output simultaneously to all of the photoelectric conversion circuits from the source of the first switch transistor.

For at least similar reasons as discussed above, Applicants respectfully submit that the combination of Koizumi, Satoshi and the AAPA does not teach, suggest or otherwise render obvious such features. Accordingly, Applicants submit that claims 22 and 23 are patentable over the cited prior art, an indication of which is kindly requested.

III. Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 13-19 are allowed.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited.

If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Shigetaka KASUGA et al.

By: Kenneth W. Fields

Kenneth W. Fields
Registration No. 52,430
Attorney for Applicants

KWF/ra/mjw
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
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